THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KYOKO IWASAWA,
TAKASHI KUROSAWA,
and SUMIO KIKUCHI

Appeal No. 1997-1212
Application 08/017,839[1]

ON BRIEF

Before THOMAS, BARRETT, and FRAHM, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

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[1] Application for patent filed February 16, 1993, entitled "Method For Supporting Parallelization Of Source Program," which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application 04-057674, filed March 16, 1992.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-12. The amendment after final rejection submitted with the Appeal Brief (Paper No. 11), which is said by the Examiner to be a duplicate of the amendment after final (Paper No. 7), has not been entered as noted in the Examiner's Answer (Paper No. 12, page 1).

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to a parallelization supporting method. When the parallelizability of the program is indeterminable, "a decision of parallelizability is made by use of assist information inputted by a user from a terminal 4, or made by actually executing the source program" (specification, page 7, lines 12-15).

Claim 1 is reproduced below.

> 1. A method for supporting parallelization, comprising the steps of:
>
> receiving data representative of a predetermined reference condition from an associated

source program into a data processing device, the data processing device including of [sic] a processor unit and a data storage;

deciding via the data processing device, based on the predetermined reference condition, whether a portion of the source program is determinable as parallelizable;

prompting, in accordance with an output of the data processing device, a user for assist information upon a determination by the deciding step that said program portion is presently indeterminable as parallelizable; and

deciding, via the data processing device, whether said program portion is parallelizable, based on assist information supplied from the user.

The Examiner relies on the following prior art:

Iwasawa et al. (Iwasawa) 5,151,991 September 29, 1992
(filed October 18, 1988)

Padua, et al. (Padua), Advanced Compiler Optimizations For Supercomputers, Communications of the ACM, Volume 29, Number 12, December 1986.

Claims 1-12 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention.

Claims 1-12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Padua and Iwasawa.

We refer to the Final Rejection (Paper No. 6) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 12) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 11) (pages referred to as "Br__") for Appellants' arguments thereagainst. The Reply Brief (Paper No. 13) received January 22, 1996, has not been entered as noted in the Letter (Paper No. 14) entered April 12, 1996, and has not been considered.

OPINION

Grouping of claims

Appellants state that "[c]laims 1-12 are directed to a method for supporting parallelization of a source program" (Br7), but does not state whether the claims stand or fall together. The Examiner states that "Appellant groups claims 1-12 as being directed to a method for supporting parallelization of a source program and therefore they all stand or fall together" (EA2). No Reply Brief has been filed.

While Appellants technically do not comply with Patent and Trademark Office rules requiring a statement that the

claims do not stand or fall together, 37 CFR § 1.192(c)(7) (1995), the Argument section of the brief does separately argue several claims in addition to claim 1, in particular, claims 5 and 10. The Examiner should have addressed these claims separately. Looking back over the prosecution history, we see that the claims have never been treated individually under 35 U.S.C. § 103. Rather than remanding the case, we address the claims on the merits based on the references.

35 U.S.C. § 112, second paragraph

The second paragraph of 35 U.S.C. § 112 requires that a claim set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure as it would be by the person of ordinary skill in the art. See Orthokinetics, Inc. v. Safety Travel Chairs, Inc., 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986). Claim breadth should not be confused with indefiniteness. See In re Miller, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971).

One source of the Examiner's problems is failing to read the claims in light of the disclosure. The Examiner

states that "a predetermined reference condition" in claim 1 is indefinite because it "is not clear what kind of condition is being referred to" (FR2) and that "based on the predetermined reference condition" in claim 1 is therefore vague (FR2-3). Appellants point to the use of the term "predetermined decision reference condition" at page 14, lines 19-25, of the specification. The Examiner states that the "condition is not fully defined in the specification" (EA15), which sounds more like a lack of enablement issue. The Examiner does not explain why the term in the claim is indefinite in view of the specification.

Another source of the Examiner's problem is confusing claim breadth with indefiniteness. For example, the Examiner states that "in accordance with an output of the data processing device" in claim 1 is vague (FR3), when it is just a very broad limitation. Similarly, the rejection that "[t]here is nothing in the claim about the criteria or parameters for parallelization" (FR3) really concerns claim breadth.

The Examiner states that "[i]t is not possible to determine whether 'via the data processing device' means the

user is making a decision or the machine is making a decision" (EA15). Appellants address this argument in connection with the patentability rejection (Br10-11). The term "via" is defined as "by means of" and indicates that part of the step of deciding must be performed by the "data processing system." However, the step of "deciding, via the data processing device, whether said program portion is parallelizable, based on assist information supplied from the user" does not exclude the user from taking some action to cause the system to perform the step, such as submitting a rewritten program and running the compiler again. The limitation is broad, not indefinite.

Still another source of the Examiner's problems is failure to properly interpret the claim language. Many of the claim limitations appear to be drafted in step-plus-function format under 35 U.S.C. § 112, sixth paragraph, because they recite a step and function (e.g., deciding . . . whether a portion of the source program is determinable as parallelizable) without reciting any acts in support thereof. This format requires that the limitations be "construed to cover the corresponding . . . acts

described in the specification and equivalents thereof," 35 U.S.C. § 112, sixth paragraph. For example, the Examiner states (FR3): "The steps of deciding are desired results. They start out by 'deciding...' but do not recite what must be done to perform these steps." Appellants argue that the language would be understood by one of ordinary skill in the art when read in light of the disclosure (Br15). The Examiner does not address how the claims are indefinite when properly interpreted under 35 U.S.C. § 112, sixth paragraph, to include the acts described in the specification.

Some of the other problems appear due to the Examiner's failure to read the claims closely. For example, the Examiner states that "[i]t is unclear when the inserting step [of claim 6] should be performed in terms of the steps of claim 5" (FR4). However, claim 6 says "the step of inserting into said source program prior to said execution," and it is clear that this means before the step of "sequentially executing said source program" in claim 5.

The Examiner notes a discrepancy in claim 6 (FR4): "regarding claim 6, the claim recites 'when it is not possible to decide' where the previous claim [5] already

stated deciding" (FR4). Claim 6 recites "said step of sequentially executing in accordance with a program statement for outputting said information when it is not possible to decide whether said program portion is parallelizable," whereas claim 5 recites "sequentially executing . . . upon a determination in the step of deciding that said program portion is parallelizable" (emphasis added). Actually, it appears that the problem lies in claim 5 rather than claim 6.

Claim 5 recites "sequentially executing said source program to generate an execution output, upon a determination in the step of deciding that said program portion is parallelizable" (emphasis added) and then "deciding . . . whether said program portion is parallelizable in accordance with the execution output." This is misdescriptive, since it recites deciding whether the program portion is parallelizable after determining that it is parallelizable. The executing step should take place when it is not possible to decide whether the program portion is parallelizable as stated in originally filed claim 5; see also specification, page 7, line 10, to page 8,

line 8. This error was introduced by the amendment received October 28, 1994 (Paper No. 5). The rejection of claim 5 and its dependent claims 6-8 under 35 U.S.C. § 112, second paragraph, is sustained.

We have considered the Examiner's other rejections in the Final Rejection and the Examiner's Answer but are not persuaded that the claims are indefinite for the reasons discussed above. The rejection of claims 1-4 and 9-12 under 35 U.S.C. § 112, second paragraph, is reversed.

35 U.S.C. § 103

The Examiner interprets (FR7-8; EA3) the claimed step of "prompting, in accordance with an output of the data processing device, a user for assist information upon a determination by the deciding step that said program portion is presently indeterminable as parallelizable" in claim 1 to correspond to the user interaction strategy in Padua where, "[w]hen something is not vectorized, the compiler gives a reason . . ." (Padua, page 1198), and "[i]f users are not satisfied with the outcome, they may resubmit the program after rewriting parts of it or after inserting directives or assertions" (Padua, page 1198). Thus, the Examiner (1)

interprets teachings for "vectorization" to apply to "parallelization," and (2) interprets the claimed "prompting" to read on the compiler giving reasons to the user and the claimed "assist information" to broadly read on the rewritten parts of the program or the inserted directives or assertions. The compiler decides whether the program portion is parallelizable based on the user entered "assist information."

Appellants acknowledge the Examiner's interpretation (Br12, first full para.), but then just states that "there is no 'prompting' or 'receiving' in an interactive environment as set forth in independent claims 1, 5, 9 and 12" (Br12). Appellants do not explain why the Examiner's interpretation is erroneous or unreasonable. The Examiner responds that a "prompt" is defined as "displayed text indicating that a computer program is waiting for input from the user" and so the user interaction in Padua involves prompts (EA11).

The step of "prompting . . . for assist information" in claim 1 is extremely broad. There is no stated reason why "prompting" cannot broadly be read on the compiler providing

reasons why a program portion was not vectorized or why the "assist information" cannot broadly be read on rewritten parts of the program or user-inserted directives or assertions which assist the compiler to vectorize the program. Claim 1 does not define the nature of the prompt or the assist information. Appellants do not contest the implied finding that the teachings with respect to user interaction for "vectorization" in Padua are applicable to "parallelization." Padua is clearly directed to parallelization. Appellants do not contest that it would have been obvious to perform the teachings of Padua on a data processor as taught by Iwasawa. We next consider Appellants' arguments why the evidence is not sufficient to establish a prima facie case of obviousness.

Appellants argue that "the subject invention teaches a system which allows for parallelization without knowledge of parallelization techniques" (Br8). The Examiner responds that the claims are broad and that the arguments do not correspond to the limitations in the claims (EA5-6). We agree with the Examiner that the arguments are not commensurate in scope with claim 1. The language of claim 1

does not preclude the user from being highly skilled in parallelization techniques. Claim 1 does not define the nature of the "prompting" as being questions. Nor does claim 1 limit in any way what is considered "assist information"; any information which would assist the compiler in parallelizing the program can be considered "assist information," including actually rewriting the program or inserting directives or assertions.

Appellants argue that the present invention "provides for a secondary, automated determination (i.e. deciding step) as to whether a particular program fragment is parallelizable after receipt of prompted, user input" (Br8). The compiler in Padua re-determines whether the program is parallelizable in response to the user inputted information. That is, the user in Padua provides information, and may provide more detailed information than in Appellants' system, but it is still the compiler that determines whether the program is parallelizable.

Appellants argue (Br9):

> The subject application teaches an automated parallelization method for use in connection with the parallelization of a source program. Unlike earlier systems, including Padua, et al., access to arguments

> and program subroutines are examined even if a loop includes a subroutine call associated with an argument. This examination provides for a decision as to whether or not the subroutine call effects a loop in parallelization . . . . In addition to the foregoing, the subject invention teaches a mechanism by which a user may be queried as necessary, concerning parallelization conditions in order to perform efficient, automatic conversion of a programmed fragment . . . . In the event a user may not answer a question, a source program that includes directives for outputting a result of program executions is automatically generated. Thereafter, the program is executed . . . . The system further performs parallelization on a basis of a result of such execution. Accordingly, the only thing a user needs to do is answer prompting questions. Specific knowledge of a parallelization technique or directives to the compiler is not required of the user.

These arguments are not persuasive because they are not supported by limitations in claim 1. Claim 1 does not recite that the parallelization examines subroutines or that the "assist information" relates to "parallelization conditions."

Appellants argue (Br9-11) that the Examiner's reasoning in the Final Rejection (at FR6, last full para. beginning with "with respect to Padua") is unclear (as indicated by the three notes, Br10), and is erroneous to the extent it states that the claim language, "via the data processing device," does not provide a limitation that the decision

regarding parallelization is accomplished by the data processing device, but might be directed to simply displaying data rather than performing the decision. The Examiner responds that he "was only pointing out that 'via the data processing device' does not mean that the user has made a decision (nor does it mean that the data processing system made a decision" (EA9). As discussed in connection with the rejection under 35 U.S.C. § 112, second paragraph, we interpret "via the data processing device" to require that the data processing system performs the step of "deciding." Nevertheless, any error in the Examiner's position does not affect the patentability rejection. Padua does not end its operation when it displays a reason why parallelization may not be accomplished as argued by Appellants (Br11). The compiler in Padua (running on a data processing device) determines whether the program is parallelizable with the user-input information entered in response to the reasons. It would not make sense for the compiler to gather information and then not use it. The step of "deciding, via the data processing device" includes the user in Padua re-running the compiler to have the

compiler decide whether the program is now parallelizable. The user does not decide in Padua.

Appellants' arguments are not persuasive of non-obviousness. The rejection of claim 1 is sustained. Dependent claims 2 and 3 have not been separately argued and, so, these claims stand or fall together with claim 1. The rejection of claims 2 and 3 is sustained. Appellants mention claim 4 (Br14), but do not provide any argument in support of patentability. See 37 CFR § 1.192(c)(7) ("Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable."). Claim 4 falls with claim 1. The rejection of claim 4 is sustained.

Independent claims 9 and 12 include limitations for analysis, receipt of user feedback, and performing subsequent analysis which correspond to claim 1. Appellants do not argue the step of "inserting . . . a program statement" (claim 9) or the step of "either inserting a program statement . . . or compiling" (claim 12) and, so, we do not address these limitations. See 37 CFR § 1.192(c)(8)(iv) (argument must address the errors

including "the specific limitations in the rejected claims which are not described in the prior art"). Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."). The rejection of claims 9 and 12 is sustained for the reasons stated with respect to claim 1. Claim 11 is not separately argued. The rejection of claim 11 is sustained.

Appellants argue (Br12-13): "Additionally, claim 10 further defines that in the step of receiving 'assist information' the 'user' is directed as to the type of assist information which is to be inputted. There is no such limitation or discussion found in Padua, et al." Although the argument is minimal, Appellants have stated that the limitations of claim 10 are not found in Padua. The Examiner quotes Appellants' argument (EA12-13), but does not address where the limitation is found. Padua gives reasons why a parallelization (vectorization) could not be accomplished, but does not direct the input of assist

information. The user is apparently free to do whatever he or she wants to solve the problem. The rejection of claim 10 is reversed.

Independent claim 5 is intended to be directed to actually executing the source program to generate assist information instead of using assist information input by a user when it is not possible to decide whether the program is parallelizable. This is described in the specification at, for example, page 7, line 10, to page 8, line 8. As noted in connection with the rejection under 35 U.S.C. § 112, second paragraph, claim 5 has a misdescriptiveness problem. However, as to the patentability rejection, we do not find anything in Padua that would have taught or suggested executing the program and then using the results of this execution in a step of deciding whether the program portion is parallelizable. The Examiner does not address the distinct limitations of claim 5. The rejection of claims 5-8 under 35 U.S.C. § 103 is reversed.

CONCLUSION

The rejection of claims 5-8 under 35 U.S.C. § 112, second paragraph, is sustained, and the rejection of claims 1-4 and 9-12 under § 112, second paragraph, is reversed.

The rejections of claims 1-4, 9, 11, and 12 under 35 U.S.C. § 103 is sustained, and the rejection of claims 5-8 and 10 under § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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